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Application Number	09/899,763
Filing Date	July 5, 2001
First Named Inventor	Meyer
Art Unit	2123
Examiner Name	Not Assigned
Attorney Docket Number	3020.02US02

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL [*]	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
ll		<i>Electronic Circuit Simulation in a Mixed-Language Environment</i> , Litovski et al., Microelectronics Journal, Mackintosh Publications Ltd., Vol. 29, No. 8, August 1, 1998; pgs. 553-558.	
ls		<i>Hardware Description Languages for ALECSIS Simulator</i> , Damjanovic et al., Microelectronics 1995 Proceedings, New York, IEEE, September 1995, pgs. 525-528.	
ls		Verilog-AMS Language Reference Manual, Open Verilog International, December 1999, Los Gatos, California, Chapter 9.	
ls		<i>On the Design of Mixed-Mode Simulators for Modern VLSI Circuits</i> , Abdallah et al., Circuits and Systems Proceedings 1995, New York, IEEE, August 1995, pgs. 1168-1171.	
ls		<i>A System-Level Simulation Environment for System-on-Chip Design</i> , Schneider et al., 13 th Annual IEEE International ASIC/SOC Conference, September 2000, Washington, D.C., pgs. 58-62.	

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